A Scan Chain Adjustment Technology for Test Power Reduction

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Abstract*

Recently test power dissipation has become a more and more challenging issue. This paper proposes a technique to solve this problem through scan chain adjustment to eliminate unnecessary transitions in scan chains. An extended WTM (EWTM) metric is proposed to estimate dynamic power dissipation in circuit under test caused by transitions in test stimulus and response vectors. And the routing overhead of this methodology can be reduced through scan chain adjustment guided with our Distance of EWTM (DEWTM) metric. Experimental results on ISCAS’89 benchmarks circuits show that the proposed approach can reduce average power dissipation during scan test by 72.2\% on average, with negligible routing overhead.

1. Introduction

The System-on-Chip (SoC) revolution has brought many new challenges to both design and test engineers. Among these challenges, the power dissipation is one of the most important issues [1]. Power dissipation may be doubled in test mode than in normal mode [2]. Several reasons cause this increased power usage: First, high toggle rate usually improve test efficiency; therefore, in the test mode the switching activity of all nodes is often several times higher than that during normal operation. On the other hand, test engineers use parallel testing in SoCs to reduce the test application time, which might result in excessive power dissipation. Finally, successive functional input vectors applied to a given circuit during system mode have a significant correlation. In contrast, the correlation between consecutive test patterns can be low. Excessive power dissipation during test threatens the reliability of the SoC being tested, hampering the test of multiple SoC cores in parallel [3]. To enhance parallelism among core tests, and hence to minimize the SoC test time, aggressive test power reduction methodologies should be developed.

Scan-based test techniques dominate the market currently, but they suffer from increasing test power dissipation. The transitions in the scan cells during shift phase, which contains both scan-in and scan-out, reflects into internal core lines, creating excessive transitions in the cores under test unnecessarily. The consequent switching activity magnifies the test power dissipated.

Many techniques that aim at scan test power reduction have been proposed recently. In [5] a technique of scan chain partitioning was proposed. The scan chain was decomposed into several partitions so as to have only one of the partitions active at a time, reducing scan chain rippling. The utilization of externally controlled gates [6, 7] was shown to reduce test power drastically, albeit at the expense of functional performance degradation due to additional gate delays introduced on functional paths. Appropriate primary input assignments during shift phase [8] helped reduce transition propagation from the scan chain to the circuit under test; however, the effectiveness of such techniques is limited. The scan cell reordering technique in [9] using a heuristic algorithm to modify the order of the scan cells within the scan chain so as to reduce switching activity. Scan chain modifications with XOR/NOT-gate insertion for test power reduction were proposed in [4, 10]. [10] investigated only stimuli transformation, but [4] considered not only stimuli but also responses transformation, therefore reduced test power during the entire shift phase.

In this paper, we will propose a low power DFT technique which can reduce test power through scan cells grouping and reordering according to both stimuli and responses information. We proposed a metric: Extended Weighted Transition Metric (EWTM) which is extended from WTM [11] to estimate the dynamic power dissipation in circuit under test caused by transitions in given test cube. A Distance of Extended Weighted Metric (DEWTM) is also proposed to estimate the co-effect of the distance between two adjacent scan cells and their EWTM on scan chain adjustment to reduce the shift power dissipation with shorter wire length. These two metrics are used to guide our scan chain adjustment procedure. The proposed
method can significantly reduce power dissipation during shift phase, with negligible routing overhead.

The rest of this paper is organized as follows. In the following section we are introducing power dissipation model of CMOS circuits and presenting our EWTM metric. The proposed scan chain adjustment algorithm is outlined in section 3. The wire routing problem of our algorithm will be solved by DEWTM in section 4. Section 5 reports experimental results obtained on the benchmark circuits. Section 6 conclude the paper.

2. Shift Power Dissipation Model

Power dissipation in CMOS circuits can be static or dynamic. Static power dissipation is caused by leakage current or other current continuously drawn from the power supply. Dynamic power dissipation occurs during output switching because of short-circuit current, and charging and discharging of load capacitance. For existing CMOS technology, dynamic power is the dominant source of power dissipation, although this might change with shrinking technology.

[11] proposed Weight Transitions Metric (WTM) to estimate the dynamic power caused by stimuli or responses transitions. Consider a scan chain of length \( l \) and a scan vector \( V_i = V_{i,1}V_{i,2}...V_{i,l} \) with \( V_{i,j} \) scanned in before \( V_{i+1,j} \), and so on. As shown in [11], the WTM of the vector is given by

\[
WTM = \sum_{i=1}^{n} (V_{i,j} \oplus V_{i,j}) \times (l-j) \tag{1}
\]

If the entire test cube contains \( N \) vectors, then the average scan-in power \( P_{\text{avg}} \) can be estimated as:

\[
P_{\text{avg}} = \sum_{i=1}^{N} \sum_{j=1}^{l} (V_{i,j} \oplus V_{i,j}) \times (l-j) / N \tag{2}
\]

Similar formulae can be applied for scan-out power estimation.

Since these formulae only focus on scan-in or scan-out power respectively, they can only describe the situation that scan-in and scan-out are serially executed. When scan-in and scan-out are executed in parallel, the toggling condition in scan chains is not as simple as illustrated in equation (1) and (2). Consider the example in Fig. 1, suppose the response vector of the \( i \)th stimulus vector is \( R_i = R_{i,1}R_{i,2}...R_{i,l} = 1110 \) and the \((i+1)\)th is \( S_{i+1} = S_{i+1,1}S_{i+1,2}S_{i+1,3}...S_{i+1,l} = 1001 \), the response vector 1110 is scanned-out bit by bit with stimulus vector 1001 scanned-in simultaneously. The parallel scan-in and scan-out period can be seen as a shift phase in scan test, while the whole test is repetitions of such phases interrupted by capture cycles.

In Fig. 1, there is one logic value difference within the vector 1110, and two logic value differences in 1001. The logic value difference in response vector causes power dissipation at 3 scan cells: \( \text{Cell}_1 \) to \( \text{Cell}_3 \), while the two differences in stimulus vector cause 3

\[
\text{Fig 1. Toggling on scan chain caused by stimulus & response transitions}
\]

(Cell1 to Cell4) and 1 (Cell5) cell to switch respectively. Notice that the logic value differences between \( R_{i,1} \) and \( R_{i,3} \), and \( S_{i+1,2} \) and \( S_{i+1,4} \) are both caused by different logic value between \( \text{Cell}_i \) and \( \text{Cell}_{i+1} \), but these differences have different effect on scan chain transitions during the shift phase. The former one causes 3 cells to toggle during scan-out, while the later one only induces \( \text{Cell}_5 \) to toggle during scan-in. There is another kind of transitions induced by different logic values between the last bit of response vector and the first bit of stimulus vector which causes power dissipation at all scan cells. We can extend the WTM metric to estimate power dissipated in scan chain caused by logic value differences within such pairs of stimulus and response vectors, we call it Extended Weighted Transition Metric (EWTM). If the test cube has \( N \) stimulus vectors and \( N \) response vectors, for two adjacent cells \( \text{Cell}_i \) and \( \text{Cell}_{i+1} \), \( \text{EWTM}_j \) caused by logic value differences between them is

\[
\text{EWTM} = \text{WTM}_{\text{scan-in}} + \text{WTM}_{\text{scan-out}} = \sum_{i=1}^{N} (S_{i,j} \oplus S_{i,j}) \times (l-j) \tag{3}
\]

\[
\text{where } 1 < j < l - 1, \text{ EWTM is the sum of WTM}_{\text{scan-in}} \text{ happened during stimuli scan-in and WTM}_{\text{scan-out}} \text{ happened during responses scan-out; When } j = l, \text{ EWTM is caused by the transition between the last bit of response vector and the first bit of next stimulus vector during the whole shift phase, which is denoted as WTM}_{\text{scan-induce scan-out}} \text{ in equation (3). This term can be reduced by test vector reordering, which is not emphasized in this paper, but is also interesting. The average power dissipation can be estimated as the following equation based on equations (2) and (3):}
\]

\[
P_{\text{avg}} = \left( \sum_{i=1}^{N} (R_{i,j} \oplus S_{i,j}) \times (l-j) \right) + \sum_{i=1}^{l} (R_{i,j} \oplus R_{i,j}) \times j \tag{4}
\]

\[
+ \sum_{i=1}^{l} (R_{i,j} \oplus S_{i,j}) \times j / N.
\]
From the equation above, we can find that the power dissipated during scan test depends not only on logic value differences within stimuli or responses respectively, but also on the weighted sum of them.

3. Scan Chain Adjustment Algorithm

In order to reduce test power dissipation as mentioned above, we should reduce transitions caused by different logic values between stimuli and responses in adjacent scan cells as many as possible.

To tackle this NP problem efficiently, the heuristic procedure operates in two steps: First, grouping the scan cells into two separate scan chains, which will be illustrated in section 3.1; second, reordering the scan cells in each group, which is described in section 3.2.

3.1 Scan Cell Grouping

Because the logic value of a scan cell is either 0, 1 or X in each vector of a test cube (consisting of both test stimuli and responses), the possibility of 0 or 1 in each scan cell is a constant value in a test cube, and X bits in test stimuli of a test cube can be assigned to either 0 or 1 without affecting the fault coverage. For example, the test cube shown in Fig. 2, there are ten scan cells in the circuit, and the test cube is consist of 5 test stimulus vectors (S1 to S5) and 5 test response vectors (R1 to R5).

The possibility of 0 and 1 of each scan cell in this test cube can be calculated according to logic value in each test vector as:

\[
P_i = \frac{\sum_{i=1}^{n} X_i = 1/0}{n}
\]

where \( n \) is the number of test vectors(include stimuli and responses) in the test cube. The possibilities of 0 and 1 in each scan cell are shown after \( P_i \) and \( P_o \) respectively in Fig. 2.

The scan cells with higher \( P_1 \) than \( P_0 \) means they are more likely to have 1 as their logic values, and the scan cells with higher \( P_0 \) means they are more likely to have 0 as their logic values. So we can group scan cells in a design into two separate scan chains according to their possibility of 0 and 1. The scan cells with higher possibility of 1 are grouped into one scan chain called Chain1, and the scan cells with higher possibility of 0 are grouped into Chain0. As shown in Fig. 2, \{Cell1, Cell2, Cell3, Cell4, Cell5\} are grouped into Chain1, and \{Cell6, Cell7, Cell8, Cell9\} are grouped into Chain0. If the possibilities of 0 and 1 of a scan cell have equal value, like the 4th scan cell in Fig.2, this scan cell will be assigned to the scan chain with fewer scan cells, and it is Chain0 in this case, for balance between these two scan chains.

After dividing scan cells into these two scan chains, the logic values of scan cells in Chain1 are more likely to be 1, while the logic values of scan cells in Chain0 are more likely to be 0. Now logic value differences among scan cells in the same scan chain will be reduced so that fewer transitions will be induced during the scan phase.

Because \( j \) in equation (4) will also be reduced through dividing one single scan chain into two, it will bring additional benefit to scan power reduction. There is also another advantage of scan chain segment that it will reduce the test time, which is not emphasized in this paper but is also a very important issue during test. The only overhead of grouping scan cells into two scan chains is a pair of scan-in and scan-out ports, which can be neglect in VLSI designs.

3.2 Scan Cell Reordering

After grouping scan cells into two individual scan chains according to their possibility of 0 and 1 as mentioned in the previous section, the order in which the scan cells in the same scan chain will be connected should be determined to minimize the occurrence of transitions in each scan chain during scan-in and scan-out operations.

The scan cells in each scan chain are reordered guided with \( EWTM \). From equation (3) we can see that for a given position, where \( j \) is constant, \( EWTM_j \) is only relative to \( \Sigma(S_{i,j} \oplus S_{j+1}) \) and \( \Sigma(R_{i,j} \oplus R_{j+1}) \), but their weights are not equivalent. \( \Sigma(S_{i,j} \oplus S_{j+1}) \) has a weight of \((i,j)\), while \( \Sigma(R_{i,j} \oplus R_{j+1}) \) has a weight of \( j \).

The first step is to find two scan cells to be put in the first two positions nearest to the scan-out port in Chain1 and Chain0. For doing this, in each scan chain we find two cells have the minimal \( EWTM_i \) between them. For the test cube example in Fig. 2, \( EWTM \) between every scan cell pair is demonstrated as weight of each edge in

**Fig 2. Possibilities of 0 and 1 of Scan Cells**

<table>
<thead>
<tr>
<th>Scan Cells: 1 2 3 4 5 6 7 8 9 10</th>
<th>S1= X X X X 1 1 1 0 X</th>
<th>R1= X X X X X X X X X X</th>
</tr>
</thead>
<tbody>
<tr>
<td>S2= 0 0 1 0 1 X 0 X X X</td>
<td>R2= 1 0 1 0 1 0 1 0</td>
<td></td>
</tr>
<tr>
<td>S3= X 0 1 1 1 1 0 1 0 1 0</td>
<td>R3= 0 1 0 1 1 1 1 1 0 1</td>
<td></td>
</tr>
<tr>
<td>S4= X 0 1 0 0 1 1 0 X X</td>
<td>R4= 1 0 1 0 0 X X X X</td>
<td></td>
</tr>
<tr>
<td>S5= X 1 1 0 1 1 1 X X X X</td>
<td>R5= 1 0 1 0 0 0 0 X X X</td>
<td></td>
</tr>
</tbody>
</table>

**P1= 0.4 0.2 0.6 0.4 0.3 0.5 0.5 0.4 0.2 0.3**

**P0= 0.2 0.5 0.3 0.4 0.5 0.2 0.3 0.1 0.5 0.2**

<table>
<thead>
<tr>
<th>Chain ID</th>
<th>1 0 1 0 0 1 1 1 0 1</th>
</tr>
</thead>
</table>

The scan cells in each scan chain are reordered according to their value differences within stimuli or responses respectively, but also on the weighted sum of them.
the cost graph in Fig.3 (a) and (b), while each vertex in these cost graphs represents for a scan cell in each scan chain. Because there is no logic value difference between Cell_6 and Cell_8, if they are put in the first two positions nearest to the scan-out port in Chain_1, EWTM_j will be 0 in this scan chain, so the first two scan cells ordered to Chain_1 are Cell_6 and Cell_8. Accordingly, X bits in test stimuli in these two cells will be assigned to 0 or 1 according to determined logic values of each other. If the logic values of the two cells are both X, they will not be assigned to 0 or 1 until the next cell being ordered into the scan chain has a determined logic value. In this example, the test stimulus bits in Cell_6 and Cell_8 will all become S_{1,6}.S_{5,6}=S_{1,8}.S_{5,8}=1X111. Similar procedure will be performed on Chain_0. Because EWTM_j between Cell_6 and Cell_8 is 2, which is the minimal among scan cells in Chain_0, these two scan cells will be put in the first two positions in Chain_0. The scan cell in the first position of the scan chain should be deleted from the cost graph. Here we assume that Cell_6 and Cell_8 are first cells of these two scan chains respectively.

After determining the first two scan cells in these two scan chains, the following steps are easier. Assuming we are ordering the j-th scan cell into the scan chain. The scan cell has minimal EWTM_{j-1} to the (j-1)th scan cell will be ordered into the scan chain next, and the (j-1)th scan cell will be deleted from the cost graph. X bits in test stimulus bits in scan cells have been ordered into a scan chain will be assigned to determined logic value of their neighbor cells. Each time after one scan cell has been ordered into a scan chain; EWTM_j between this scan cell and the scan cells haven’t been ordered into the scan chain should be calculated and updated as the new weight of each edge in the new cost graph.

For example in Fig.3(a). After put Cell_6 as the first scan cell in Chain_1, it will be deleted from the cost graph, and EWTM_2 between Cell_6 and all other scan cells will be calculated and updated as the new weight of each edge in the cost graph, as shown in Fig.4. From Fig.4 we can see EWTM_2 between Cell_1 and Cell_6 is minimal, so Cell_1 is the next scan cell to be ordered into Chain_1. Now test stimuli in Cell_1, Cell_6 and Cell_8 will become S_{1,1}.S_{5,1}=S_{1,6}.S_{5,6}=S_{1,1}.S_{5,1}=111111. Such computation will be repeated until all scan cells grouped into Chain_1 have all been ordered into it. Similar procedure will also be performed in Chain_0, to get the order in which scan cells are connected in Chain_0.

4. Wire Routing Consideration

Because of the localization of each scan cell in a design, there’s a wire routing problem during our scan cell reordering process. It can not guarantee short scan connections. To tackle this problem, we also propose a solution that can design low power scan chains with low wire length overhead.

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**Fig 3. Cost graph**

(a) Cost graph of scan cells in Chain_1 with EWTM_j

(b) Cost graph of scan cells in Chain_0 with EWTM_0

**Fig 4. New cost graph of scan cells in Chain_1**

To guarantee short scan wire connection, we should reorder the scan cells considering not only the transitions number induced by logic value differences between them, but also the distance between them.

Firstly, placement information of each scan cell can be got using EDA tools, such as Encounter developed by Cadence Corporation. Secondly, the distance D_{i,j} between each pair of scan cells will be calculated as:

\[ D_{i,j} = \sqrt{(X_i - X_j)^2 + (Y_i - Y_j)^2} \]  

where X_i and Y_i are x-coordinates of these two scan cells, Y_j and Y_j are y-coordinates of them.

Thirdly, a new metric: Distance of Extended Weighted Transition Metric (DEWTM) is proposed to estimate the co-effect of cell distance and transitions number caused by logic value differences in test stimulus and response vectors. If we are ordering the (j+1)th cell into the scan chain, DEWTM_j between the j-th cell in the scan chain and all other scan cells that have not been ordered into the scan chain is:

\[ DEWTM_j = D_{i,j} \times (EWTM_{j} + 1) \]  

where i ranges all the scan cells that have not been ordered into the scan chain now.

Finally, in new reordering procedure considering wire routing problem, the scan cell has the minimal DEWTM_j will be ordered into the scan chain next. Because EWTM_j can be 0 in more than one scan cells sometimes, the scan cell has the shortest distance to the j-th cell among them should be ordered into the scan chain next. Using DEWTM to guide our scan cell reordering procedure will guarantee fewer transitions happened in scan chain with shorter wire connection among scan cells.
5. Experimental Results

Two sets of experiments have been conducted on full-scan version of several ISCAS’89 benchmark circuits using different scan chain adjustment methodologies. One is performed without considering the wire routing problem; the other one does consider the wire length using our DEWTM metric. These two sets of experiments are described in details in the following sections. MinTest [12] test cubes are used to compute the test power reductions achieved by the proposed methodologies. Table 1 presents general information about the benchmarks and test cubes used to evaluate our scheme: the number of scan cells, test vectors and X bit percent are all provided.

5.1 Experiments without considering wire routing problem

Table 2 demonstrates the power reduction results when the scan cell grouping and reordering algorithm without consideration of wire routing are implemented in the scan chain. The values of EWTM during the shift of the test data are provided. The original EWTM values are list under “Original”. There are two scan chain specification modes: one use a single scan chain, the other use two scan chains. The EWTM value of these two modes are list under “ChainCnt1” and “ChainCnt2” respectively. The values of EWTM using our algorithm are list under “Proposed”. And the EWTM reduction of our method compared to different original scan design are list under “Reduction”, while reduction compared to single scan chain are list under “ChainCnt1” and that compared to two scan chains are list under “ChainCnt2”.

We have also list the shift power reduction using methodology with XOR gate insertion in [4] under “Power Reduction in [4]”, and the area overhead of method in [4] under “Area Cost in [4]”.

From Table 2 we can see that very high percentage of shift power reduction can be achieved through the proposed algorithm, it can reduce power dissipation compared to single scan design by 93.6% on average, and 88.4% compared to designs with two scan chains, which is much higher than [4]. Compared to the area overhead brought by the XOR gates in [4], our method need no additional hardware and no area overhead, but it brings wire routing problem. The wire length overhead is list in Table 3 to demonstrate this problem. Encounter developed by Cadence is used to reorder the scan design has two scan chains with high effect to achieve the relatively shortest wire length and also used to estimate the total length of a circuit under test. In Table 3, the total length of each design in different ordering method is list under “Reordered” and “Proposed” respectively. The wire length increments of our methodology compared to the reordered scan chain using Cadence Encounter are list under “Increment”.

5.2 Experiments with consideration of wire routing problem

Because the previous methodology can cause long wire connection which is not acceptable sometimes as shown in Table 3, we need do our scan chain adjustment considering wire routing problem. The percentage of EWTM reduction and wire length increment using this algorithm compared to scan design reordered by Cadence Encounter are list under “EWTM reduction” and “Wire length increment” respectively in Table 4. The EWTM reductions are also compared to two scan specification of original scan: single scan chain and two scan chains.

We can see from Table 3 and 4 that the wire length can be reduced by 17.4% on average compared to the previous algorithm. Notice that the wire lengths of s13207 and s38584 are even shorter than the wire length through reordering by Encounter without shift power reduction. Notice that the wire length of s38417 is also very long compared to that of scan chain reordered by Encounter, which may be caused by high DFF number and low X bit percentage in this circuit. But we can also see that the wire length of this circuit using our methodology with wire routing consideration is much shorter than the previous methodology without wire routing consideration.

From Table 2, 3 and 4 we can see that the wire length reduction can be achieved through shift power increment, so tradeoff should be made to decide which is more important: power dissipation or wire length. Then proper scan chain adjustment can be conduct to meet the requirement.

6. Conclusion

We addressed the test power issues in scan-based environments where this problem is more acute due to the scan chain transitions during the shift of test data in this paper. The methodology proposed in this paper aims at reducing scan chain transitions during shift cycles, significantly decreasing the circuit switching that these transitions reflect into otherwise. The wire routing problem of our methodology is also incorporated into the proposed algorithm to achieve significant power reduction with shorter wire length.
### Table 3. Wire length overhead of scan chain adjustment without consideration of wire routing

<table>
<thead>
<tr>
<th>Circuit</th>
<th>Reordered(um)</th>
<th>Proposed(um)</th>
<th>Increment (%)</th>
</tr>
</thead>
<tbody>
<tr>
<td>s5378</td>
<td>8.510e+04</td>
<td>1.010e+05</td>
<td>18.7</td>
</tr>
<tr>
<td>s9234</td>
<td>1.340e+05</td>
<td>1.544e+05</td>
<td>15.2</td>
</tr>
<tr>
<td>s13207</td>
<td>2.892e+05</td>
<td>3.362e+05</td>
<td>16.3</td>
</tr>
<tr>
<td>s15850</td>
<td>2.967e+05</td>
<td>3.460e+05</td>
<td>16.6</td>
</tr>
<tr>
<td>s38417</td>
<td>6.138e+05</td>
<td>9.502e+05</td>
<td>54.8</td>
</tr>
<tr>
<td>s38584</td>
<td>9.595e+05</td>
<td>1.324e+06</td>
<td>38.0</td>
</tr>
</tbody>
</table>

### Table 4. Percentage of EWTM reduction and wire length increment considering wire routing (%)

<table>
<thead>
<tr>
<th>Circuit</th>
<th>Transition reduction</th>
<th>Wire length increment</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>ChainCnt1</td>
<td>ChainCnt2</td>
</tr>
<tr>
<td>s5378</td>
<td>75.1</td>
<td>56.3</td>
</tr>
<tr>
<td>s9234</td>
<td>75.2</td>
<td>51.0</td>
</tr>
<tr>
<td>s13207</td>
<td>74.8</td>
<td>49.6</td>
</tr>
<tr>
<td>s15850</td>
<td>69.0</td>
<td>47.8</td>
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<td>s38417</td>
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<td>37.7</td>
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<tr>
<td>s38584</td>
<td>70.7</td>
<td>44.4</td>
</tr>
</tbody>
</table>

Two metrics have been proposed to guide the scan chain adjustment procedure. Extended Weighted Transition Metric (EWTM) is used to estimate transitions caused by different logic values between both test stimulus and response bits in two adjacent scan cells with information of their location. While Distance of Extended Weighted Transition Metric (DEWTM) is used to estimate the co-effect of distance between two adjacent scan cells and their EWTM on both scan power and wire length reduction.

Experimental results show that the scan chain adjustment methodology without consideration of wire routing can achieve shift power reduction by 93.6% on average, and 72.2% on average using algorithm considering wire routing with negligible routing overhead. So tradeoffs can be made to decide whether to consider routing constraint in adjustment of scan chains.

### References


### Table 2. EWTM reduction using scan chain adjustment method without wire routing consideration

<table>
<thead>
<tr>
<th>Circuit</th>
<th>Original EWTM</th>
<th>Proposed EWTM</th>
<th>Reduction</th>
<th>Power reduction in [%]</th>
<th>Area Cost in [%]</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>ChainCnt1</td>
<td>ChainCnt2</td>
<td>ChainCnt1 (%)</td>
<td>ChainCnt2 (%)</td>
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<tr>
<td>s5378</td>
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<td>s15850</td>
<td>5708432</td>
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<td>97.0</td>
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<td>73.4</td>
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